BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL FOR FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant Claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($) 330.00

Complete if Known	
Application Number	09/285,899
Filing Date	April 8, 1999
First Named Inventor	Shunpei YAMAZAKI et al.
Examiner Name	T. Ton
Group Art Unit	2871
Attorney Docket No.	0756-1950

METHOD OF PAYMENT

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 50-2280

Deposit Account Name: Robinson Intellectual Property Law Office

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 and credit overpayments

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☒ **Payment Enclosed:**

☒ Check ☐ Credit Card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

		Extra Claims	Fee from below	Fee Paid
Total Claims	-20** =		X $18 =	
Independent Claims	-3** =		X $86 =	
Multiple Dependent			=	

Large Entity Fee Code	Large Entity Fee	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	465	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	$330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.29(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify) Certificate of Correction					

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 6-7-2004 Andrea M Stamper

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	Eric J. Robinson	Registration No. *(Attorney/Agent)*	38,285	Telephone	(571) 434-6789
Signature				Date	6-7-04

AF/2871/$
IFW

PTO/SB/21 (08-00)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	09/285,899
Filing Date	April 8, 1999
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2871
Examiner Name	T. Ton
Attorney Docket Number	0756-1950

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☒ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosures
  1.
  2.
  3.
  4.
  5.
  6.

Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Eric J. Robinson, Reg. No. 38,285 Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, VA 20165
Signature	
Date	6-7-04

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

Type or printed name			
Signature	Adam Stamper	Date	6.7.2004

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2871
Shunpei YAMAZAKI et al.	)	Examiner: T. Ton
Serial No. 09/285,899	)	CERTIFICATE OF MAILING
Filed: April 9, 1999	)	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 6.7.2004.
For: ELECTRO-OPTICAL DEVICE HAVING LEVELING FILM	)	Adele M Stamper

APPEAL BRIEF

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. § 134 and 37 C.F.R. § 1.192(a), the Appellants submit this Appeal Brief in triplicate to appeal the examiner's final rejection of claims 9-16, 21-24, 33-36, 50-52, 54 and 57-97 in the Official Action mailed November 4, 2003.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The named inventors have assigned all ownership rights in the pending application to Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036, Japan, which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

The appellants, their legal representatives, and the assignee are not aware of any other pending appeals or interferences which will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 9-16, 21-24, 33-36, 50-52, 54 and 57-97 are pending in the present application, of which claims 9, 13, 21, 33, 57-59, 66, 69, 73, 77, 81, 85, 89 and 93 are independent. No claims have been deemed allowable by the examiner.

IV. STATUS OF AMENDMENTS

A *Supplemental Amendment* is submitted herewith in response to the Final Official Action mailed November 4, 2003. The *Supplemental Amendment* corrects minor typographical errors in the claims. It is respectfully that the *Supplemental Amendment* places the claims in better condition for appeal, does not raise any new issues that would require further consideration or search and thus is believed to be appropriate for entry after final.

Also, the *Supplemental Amendment* requests that a signed and legible copy of the Form PTO-1449 filed September 6, 2002, be sent to indicate the consideration of the references cited therein.

Further, the *Supplemental Amendment* requests consideration of the Information Disclosure Statements which were properly and timely filed on August 26, 2003, and April 5, 2004.

All prior amendments are believed to have been entered in the present application. Thus, the status of the claims in this application, including the amendments included in the attached *Supplemental Amendment*, is as set forth above and in Appendix A.

V. SUMMARY OF THE INVENTION

The present invention relates to a device, a television (e.g. Figure 9), a projector (e.g. Figure 17), or a portable computer (e.g. Figure 20), having at least one liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)), the liquid crystal panel comprising a first substrate (e.g. 50) having an insulating surface; a second substrate (e.g. 80) being opposed to the first substrate; at least one thin film transistor (TFT)/semiconductor element (e.g. 63 or 64) being formed over the first substrate, the TFT/semiconductor element including at least a channel region, source and drain regions (e.g. 55, 56 or 59, 60) with the channel region therebetween, a gate insulating film (e.g. 65) adjacent to the channel region and a gate electrode (e.g. 66 or 67) adjacent to the channel region with the gate insulating film interposed therebetween; where the channel region, the source and drain region of the one TFT/semiconductor element is formed in a semiconductor island; an organic resin/leveling film (e.g. 77) formed over the first substrate to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering the TFT/semiconductor element; a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the TFT/semiconductor element through an opening (e.g. Figure 7(H); page 14, lines 28-29; formed by mask P7) formed in the organic resin/leveling film; a liquid crystal material having ferroelectricity or antiferroelectricity (e.g. page 36, lines 2-6) and being formed between the first substrate and the second substrate; and an opposed electrode (e.g. 90) formed over the second substrate and opposed to the pixel electrode with the liquid crystal material interposed therebetween. When the device is a television (e.g. Figure 9), the television further comprises a tuner (e.g. 223) for receiving television radio waves; and the liquid crystal panel is operationally connected to the tuner.

VI. STATEMENT OF ISSUES

Whether claims 9-16, 21-24, 33-36, 50-52, 54 and 57-97 are not *prima facie* obvious based on the combination of U.S. Patent No. 5,227,900 to Inaba et al. and Japanese Patent Application Publication No. JP 61-141174 to Takeshita et al.

VII. GROUPING OF CLAIMS

The rejected claims shall stand or fall together.

VIII. ARGUMENTS

Paragraph 1 of the Official Action rejects claims 9-16, 21-24, 33-36, 50-52, 54 and 57-97 as obvious based on the combination of U.S. Patent No. 5,227,900 to Inaba et al. and Japanese Patent Application Publication No. JP 61-141174 to Takeshita et al., and refers to the Official Action dated June 5, 2001. The Appellants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

As noted in MPEP § 2142, the initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). It is respectfully submitted that Inaba and Takeshita fail to expressly or impliedly suggest all the features of the independent claims of the present invention. It is further submitted that the Examiner has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Inaba and Takeshita or to combine reference teachings to achieve the claimed invention. The present invention is directed to a liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)) comprising an organic resin/leveling film (e.g. 77) formed over a first substrate (e.g. 50) to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering a TFT/semiconductor element (e.g. 63); and a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the TFT/semiconductor element through an opening (e.g. Figure 7(H); page 14, lines 28-29; formed by mask P7) formed in the organic resin/leveling film. The prior art does not contain sufficient motivation to teach or suggest to one of ordinary skill in the art at the time of the invention that it would have been obvious to combine Inaba and Takeshita in order to form a liquid crystal panel comprising an organic resin/leveling film formed over a first substrate to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering a TFT/semiconductor element; and a pixel electrode formed on the leveled upper surface, the pixel electrode being electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film.

Inaba (Figure 5) appears to teach a substrate 30a, a gate electrode 34 on the substrate 30a, an insulating film 32 on the gate electrode 34, a semiconductor film 26 on

the insulating film 32, a source 18 and a drain 21 of a TFT on the semiconductor film 26, a pixel electrode 22 in the same layer as the drain 21 of the TFT, and an insulating layer 23b covering all the features noted above. The Official Action concedes that Inaba does not teach "the organic resin film leveling layer and the pixel electrode formed on top of the leveling layer" (page 2, Paper No. 21). The Appellants further submit that Inaba does not teach or suggest an organic resin/leveling film formed over a first substrate 30a to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering a TFT/semiconductor element 18, 21, 26, 32 and 34. Although Inaba teaches a pixel electrode 22, Inaba does not teach or suggest that the pixel electrode 22 be formed on a leveled upper surface, or that the pixel electrode is electrically connected to the TFT/semiconductor element 18, 21, 26, 32 and 34 through an opening formed in the organic resin/leveling film.

The Appellants respectfully submit that in order to render obvious the present invention, it appears that the Official Action would have to somehow find motivation to separate pixel electrode 22 from drain 21, to insert an organic resin/leveling film between the TFT 18, 21, 26, 32 and 34 and the pixel electrode 22 which covers the TFT 18, 21, 26, 32 and 34, to form an opening in the organic resin/leveling film, and to connect the pixel electrode 22 to the TFT 18, 21, 26, 32 and 34 through the opening. For reasons noted in detail below, Takeshita and the knowledge available to one of ordinary skill in the art do not contain sufficient motivation for all of the steps required to convert the device of Inaba into a device which renders obvious the present invention.

Takeshita (Figure 1(a)) appears to teach a solid state image pickup device comprising an insulating substrate 101, a nondoped polycrystalline silicon layer 102 and an interlayer insulating film 104 on the substrate 101, a gate electrode 103 in the interlayer insulating film 104 and over the silicon layer 102, a polyimide resin 106 on the interlayer insulating film 104, a contact hole in the interlayer insulating film 104 and the polyimide resin 106, and a conductive thin film 107 formed in the contact hole and apparently in contact with the nondoped polycrystalline silicon layer 102.

The Official Action asserts that Takeshita teaches "that the usual way of forming a TFT is by forming a leveling layer" (page 2, Paper No. 21). This is a mischaracterization of Takeshita. Rather, Takeshita states that "[u]sually, poly-silicon

TFTs are formed by the above mentioned method" (page 3, translation of Takeshita). The Appellants respectfully submit that Takeshita teaches that a solid state image pickup device comprises TFTs, and that TFTs for a solid state image pickup device include a polyimide resin 106 "for leveling as an interlayer insulating film" (Id.). In any event, just because Takeshita states that TFTs are usually formed by a method which includes a polyimide resin 106, this certainly does not in and of itself teach how or why a polyimide resin 106 would be incorporated into the Inaba device. Specifically, the mere teaching of a polyimide resin 106 in Takeshita does not teach one of ordinary skill in the art at the time of the invention to modify the Inaba device by separating pixel electrode 22 from drain 21, inserting the polyimide resin 106 of Takeshita between the TFT 18, 21, 26, 32 and 34 and the pixel electrode 22 which covers the TFT 18, 21, 26, 32 and 34, to form an opening in the organic resin/leveling film, and connecting the pixel electrode 22 to the TFT 18, 21, 26, 32 and 34 through the opening.

Also, it is noted that Inaba is a fully functional device. The statement in Takeshita that "usually, poly-silicon TFTs are formed by the above mentioned method" does not provide one of ordinary skill in the art with sufficient motivation to modify the fully functional Inaba device, particularly absent any disclosure or suggestion of any advantage to be achieved by such modification. It is respectfully submitted that the broad assertion that TFTs are "usually" formed in this fashion completely fails to provide a convincing line of reasoning as to why one of ordinary skill in the art would have been motivated to modify Inaba as proposed.

Further, Inaba was published in 1993 and Takeshita was published in 1986. Clearly, Inaba et al. were aware of the teachings of Takeshita et al. in 1993. If it were important to Inaba et al. to have a leveling layer in a liquid crystal device, particularly one formed between a TFT and a pixel electrode, then why is Inaba silent as to the importance of such feature? The Appellants respectfully submit that no such teaching is provided in Inaba, because it was not obvious at the time of the invention that it would have been desirable to provide a liquid crystal panel with a leveling layer formed between a TFT and a pixel electrode of the liquid crystal panel.

The Official Action further asserts that "it would have been obvious ... to combine the leveling layer of Takeshita et al with the ferroelectric display of Inaba et al

since, as taught by Inaba et al, this was well known" (Id.). Specifically, it appears that the Official Action is asserting that combining the leveling layer of Takeshita with the ferroelectric display of Inaba was well known. Nothing in the prior art supports this assertion. The Official Action has not provided any specific teaching from either Inaba or Takeshita to indicate how or why one would of ordinary skill would have been motivated to combine the teachings of Inaba and Takeshita. Specifically, it is not clear how or why one might separate the pixel electrode 22 and the drain 21 of Inaba, insert the polyimide resin 106 of Takeshita between the TFT 18, 21, 26, 32 and 34 and the pixel electrode 22 of Inaba, form an opening as taught in Takeshita in the proposed combined device, and connect the pixel electrode 22 of Inaba to the TFT 18, 21, 26, 32 and 34 via the opening of Takeshita. In Inaba, it appears that the source 18, drain 21 and pixel electrode 22 are formed in the same layer. It is not clear from Takeshita why one of ordinary skill in the art would have been motivated to divide this layer of Inaba, much less add the additional components from the Takeshita device to the Inaba device. The Official Action relies on a broad assertion that this is all "well known" without providing any specific teaching to support the assertion.

Also, as noted in the Appellants' *Amendment* filed March 13, 2001, and again in the Appellants' *After Final Amendment* filed October 5, 2001, Inaba and Takeshita fail to appreciate the problem caused by the narrow cell gap of the ferroelectric liquid crystal (FLC) or anti-ferroelectric liquid crystal (AFLC) display device, and the materiality of the flatness of the inside surface of the substrate in the FLC/AFLC display. The Official Action responded to these arguments only by stating that limitations from the specification are not read into the claims (page 2, Paper No. 26). This misses the point. As noted above, the organic resin film or leveling film of the independent claims of the present invention is formed over the first substrate in order to provide a leveled upper surface over the first substrate. Inaba does not discuss the problem caused by the narrow cell gap, and the materiality of the flatness of the inside surface of the substrate in the FLC/AFLC display, and, as noted above, there is no motivation in Inaba or Takeshita to modify the Inaba device to include such a feature. Reconsideration of the rejection of the independent claims is respectfully requested.

Further, it should be noted that the mere fact that references can be combined or

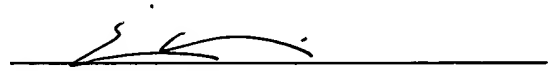
modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680 (Fed. Cir. 1990). In other words, simply because the references can be combined does not mean that they should be combined. Thus, simply because one could combine and modify the teachings of Inaba and Takeshita, does not mean one of skill in the art would do so absent some suggestion of the desirability of doing so.

In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

The present application is believed to be in condition for allowance and favorable reconsideration is respectfully requested. If the Examiner feels further discussions would expedite prosecution of this application, he is invited to contact the undersigned.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

IX. APPENDICES

A. Claims involved in the appeal.

B. U.S. Patent No. 5,227,900 to Inaba et al.

C. Japanese Patent Application Publication No. JP 61-141174 to Takeshita et al. and full English translation thereof.

APPENDIX A

PENDING CLAIMS

9. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

10. A device according to claim 9, wherein said organic resin film comprises polyimide.

11. A device according to claim 9, wherein said pixel electrode is transparent.

12. A device according to claim 9, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

13. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one semiconductor element being formed over the first substrate, said semiconductor element including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one semiconductor element is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said semiconductor element;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said semiconductor element through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate, and

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

14. A device according to claim 13, wherein said organic resin film comprises polyimide.

15. A device according to claim 13, wherein said pixel electrode is transparent.

16. A device according to claim 13, wherein said semiconductor element is a top-gate type thin film transistor in which said gate electrode is located above said channel region.

21. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

22. A television according to claim 21, wherein said organic resin film comprises polyimide.

23. A television according to claim 21, wherein said pixel electrode is transparent.

24. A television according to claim 21, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

33. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

34. A portable computer according to claim 33, wherein said organic resin film comprises polyimide.

35. A portable computer according to claim 33, wherein said pixel electrode is transparent.

36. A portable computer according to claim 33, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

50. A device according to claim 9, wherein the semiconductor island is a crystalline semiconductor island.

51. A device according to claim 13, wherein the semiconductor island is a crystalline semiconductor island.

52. A television according to claim 21, wherein the semiconductor island is a crystalline semiconductor island.

54. A portable computer according to claim 33, wherein the semiconductor island is a crystalline semiconductor island.

57. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain region of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

58. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

59. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

60. A device according to claim 57, wherein said semiconductor island is a crystalline semiconductor island.

61. A device according to claim 57, wherein said pixel electrode is transparent.

62. A television according to claim 58, wherein said semiconductor island is a crystalline semiconductor island.

63. A television according to claim 58, wherein said pixel electrode is transparent.

64. A portable computer according to claim 59, wherein said semiconductor island is a crystalline semiconductor island.

65. A portable computer according to claim 59, wherein said pixel electrode is transparent.

66. A projector having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region

and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

67. A projector according to claim 66, wherein said semiconductor island is a crystalline semiconductor island.

68. A projector according to claim 66, wherein said pixel electrode is transparent.

69. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having anti-ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

70. A device according to claim 69, wherein said organic resin film comprises polyimide.

71. A device according to claim 69, wherein said pixel electrode is transparent.

72. A device according to claim 69, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

73. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having anti-ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

74. A television according to claim 73, wherein said organic resin film comprises polyimide.

75. A television according to claim 73, wherein said pixel electrode is transparent.

76. A television according to claim 73, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

77. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with

said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having anti-ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

78. A portable computer according to claim 77, wherein said organic resin film comprises polyimide.

79. A portable computer according to claim 77, wherein said pixel electrode is transparent.

80. A portable computer according to claim 77, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

81. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain region of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

82. A device according to claim 81, wherein said pixel electrode is transparent.

83. A device according to claim 81, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

84. A device according to claim 81, wherein said semiconductor island is a crystalline semiconductor island.

85. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

86. A television according to claim 81, wherein said pixel electrode is transparent.

87. A television according to claim 81, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

88. A television according to claim 81, wherein said semiconductor island is a crystalline semiconductor island.

89. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

90. A portable computer according to claim 89, wherein said pixel electrode is transparent.

91. A portable computer according to claim 89, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

92. A portable computer according to claim 89, wherein said semiconductor island is a crystalline semiconductor island.

93. A projector having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

94. A projector according to claim 93, wherein said semiconductor island is a crystalline semiconductor island.

95. A projector according to claim 93, wherein said pixel electrode is transparent.

96. A projector according to claim 66, wherein said leveling film comprises organic resin.

97. A projector according to claim 93, wherein said leveling film comprises organic resin.

JAPAN PATENT OFFICE (JP)
PATENT APPLICATION PUBLICATION
PATENT PUBLICATION OFFICIAL REPORT (A)
SHO61-141174
Int. Cl. 4 H 01 L 27/14, H 04 N 5/335
IDENTIFICATION NUMBER:
IN-OFFICE SERIAL NUMBER : 7525-5F, 8420-5C
PUBLICATION: June 28, 1986
SUBSTANTIVE EXAMINATION: NOT REQUESTED
THE NUMBER OF INVENTION: 1 (total 4 pages)

---

1. Title of the Invention: Solid state image pickup device
Patent Application Sho 59-263366
Application December 13, 1984

2. Inventor(s)
Address: 3-3-5, Yamato, Suwa-shi
Suwa Seiko-sha
Name: Tetsuyoshi TAKESHITA

Address: 3-3-5, Yamato, Suwa-shi
Suwa Seiko-sha
Name: Hajime KURIHARA

Address: 3-3-5, Yamato, Suwa-shi
Suwa Seiko-sha
Name: Hideaki OKA

Address: 3-3-5, Yamato, Suwa-shi
Suwa Seiko-sha
Name: Kazumasa HASEGAWA

3. Applicant
Address: 2-4-1, nishi-shinjyuku, Shinjyuku-ku, Tokyo
Name: SEIKO EPSON CORPORATION

4. Attorney
Patent attorney: Tsutomu MOGAMI

SPECIFICATION

1. Title of the Invention

Solid state image pickup device

2. Scope of Claim for Patent

1. A solid state image pickup device of a type of detecting an amount of stored/discharged charges by a light receptive element formed on an insulating substrate, characterized in that a capacitor is provided with an upper electrode in parallel with said light receptive element by oxidizing a portion of a lower electrode of the light receptive element.

2. The solid state image pickup device according to claim 1 characterized in that an amorphous silicon is used as the light receptive element, chromium or aluminum is used as the lower electrode and an additional capacitance of an oxide film is formed simultaneously with phothoetching the amorphous silicon film.

3. Detailed Description of the Invention

"Field of the Invention in Industry"

The present invention relates to a solid state image pickup device utilizing solid state image pickup elements.

"Prior art"

Conventionally, CCD type or MOS type is practicable as a solid state image pickup element. In compared with an image pickup tube, the solid state image pickup element is proof against vibration and clash. The solid state image pickup element is characterized in very little power consumption to be used for a long span. Further, MOS type has bigger numerical aperture and has no limit of the amount of transfer charge compared to CCD type, so that a lot of signal can be output. However, MOS type has a defect of occurring a great noise. Fig. 3 shows a drawing of typical MOS type circuit. Referring to the drawing, the cause of noise occurrence will be described. The noise is caused by horizontal MOS FET switch which opens or closes a circuit. It is most serious problem, which causes in the case that a wiring capacitance on vertical lines V_1 to V_n is large and electrode- substrate capacitance of transistors formed on V_1 to V_n is large, so that noise charge which remains on the lines is read out. There is no comparison between the amount of noise and the capacitance of

the receptive portion, so that the S/N ratio is considerably decreased. In addition to the above mentioned problem of noise, there is one more problem of smear for both CCD type and MOS type. One of reasons is due to occurrence charge caused by light, which is incident upon the other portion in addition to the receptive portion, is signal lines.

Therefore, elements in thin film form is formed by utilizing an insulator as a substrate, so that wiring capacitance is considerably reduced. Further, S/N ratio is increased by forming additional capacitor on the receptive element. For example, as the additional capacitor, a thin film such as SiO_2 or Y_2O_3 is deposited in addition.

"Problem To Be Solved by The Invention"

However, in the above mentioned prior art, an additional thin film has to be formed in order to connect a receptive element with an additional capacitor. Therefore, process steps will increase to cause cost up. As a result, noise will be caused because a thin film will not be formed uniformly.

Therefore, the present invention will solve the problem. An object of the present invention is to provide a solid state image pickup device having an additional capacitor with high evenness in parallel with the receptive element without increasing the process steps.

"Means To Solve The Problem"

The solid state image pickup device in the present invention is characterized in that the additional capacitor with high evenness can be easily formed in parallel with the receptive element by a method wherein a part of lower electrode of receptive element is oxidized by utilizing receptive element portion as a mask to provide a capacitor between upper and lower electrodes.

In particular, the present invention is utilized an oxidation film formed by a method wherein receptive element is performed photoetching by the technique of dry etching using Freon gas comprising oxygen. Moreover, the present invention utilizes an amorphous silicon for the portion of receptive element and a polycrystalline silicon for the drive portion, respectively. Through these procedures, the solid state image pickup device having small amount of smear can be formed increasing sensitivity and saturated light quantity.

"Performance"

According to the above mentioned structure in the present invention, an oxidation film formed on lower electrode of a receptive element will be

an additional capacitor between lower electrode and upper electrode. As a result, the solid state image pickup element having small noise will be formed increasing saturated light quantity and S/N ratio.

"Example"

Fig. 1 shows a configuration drawing in accordance with the present example of the present invention. Any receptive element or switching element can be used for a semiconductor substrate. In the present invention, an amorphous silicon photodiode is used as a receptive element, and poly-silicon TFT is used as a switching element, respectively. Fig. 2 shows an equivalent circuit of Fig. 1. In Fig. 1, (a) shows a cross sectional view and (b) shows a plan view. Process steps will be described as follows. A non-doped polycrystalline silicon layer 102 is formed on an insulating substrate 101 such as quartz glass and after forming a gate insulating film by thermal oxidation, a second polycrystalline silicon 103 to be a gate electrode is formed to be also a gate line. Subsequently, ion is implanted to provide a source and drain electrode. Then, after forming SiO_2 or the like as an interlayer insulating film 104, a contact hole is formed and a vertical line 105 is formed with a conductive material such as Al, upon which a polyimide resin or the like 106 is formed for leveling as an interlayer insulating film. Usually, poly-silicon TFTs are formed by the above mentioned method. Significant process steps according to the present invention will be described as follows. After forming a contact hole on the interlayer insulating film, a conductive thin film 107 is formed by using such as Cr or Al as lower electrode of pixel. This conductive thin film 107 should be easily oxidized and the oxide film should be high resistivity and dense since it is oxidized after the formation of the receptive film 108 using the receptive film(a photo resist may be disposed thereon) as a mask in order to form an additional capacitor. As an oxidation method, it can be considered various kinds of method, however, in case that a receptive film 108 is etched by plasma using oxygen and Freon, an oxidation film 109 is formed as a necessary result, so that there is no need to add oxidation process. After oxidation by the method, oxide plasma treatment may be further conducted, or oxidation with thermal nitric acid or steam oxidation may be conducted. Table 1 shows a characteristic example of forming a lower electrode 107 by using oxidation of Cr and Al-Si and in accordance with the present example. Here, the receptive film thin 108 is an amorphous silicon (referred to a-Si, hereinafter) formed by GD plasma CVD,

and 110 may be any transparent conductive electrode (upper electrode), here, ITO.

Table 1

CONDITION	ELEMENT CAPACITY (pF/100 μ m^2)	INSULATION PROPERTY
(1) a-Si is etched by using CF_4 +O_2	0.2	good
(2) O_2 plasma treatment in addition to (1)	0.5	best
(3) thermal nitrate treatment in addition to (1)	0.5	good
(4) using Al-Si as electrode with condition (2)	0.2	regular
(5) oxidation by steam using Al-Si as electrode	0.3	good

Note) An electrode used in conditions (1) to (3) is Cr.

In the table 1, an amount of the element capacity is calculated by adding capacitance of a-Si to additional capacitor of an oxidation film. The capacitance of a-Si is approximately 0.01pF/100 μ m^2. Regarding to the uniformity, the condition (3) is best of all. Under the condition (3), dispersion of all elements is within a range of $\pm$ 1%, and under the other conditions, it is within a range of $\pm$ 2.5%. In any way, it is easier than the case of forming SiO_2 or dielectric thin film in additional process and probability of dispersion is small. (in case of SiO_2, the dispersion is within a range of $\pm$ 5%)

Referring to the equivalent circuit in Fig. 2, through the above mentioned process, the circuit is provided with an additional capacitor Ca in parallel with the receptive element Dil.

Moreover, metal is used as a lower electrode in the above mentioned example. Instead of using the metal, by using low resistance amorphous silicon which is doped impurities, an oxidation may be performed to form SiO_2 in order to use the SiO_2 as an additional capacitor.

"The effect of the Invention"

As mentioned above, according to the present invention, since the additional capacitor having a high uniformity can be formed extremely

easily and inexpensively without increasing the process steps by using the pattern of a thin film receptive element as a mask, it is possible to easily obtain excellent solid image pickup devices with low cost having a large S/N ratio and a large saturated light quantity.

4. Brief Explanation of The Drawings

Fig. 1 is example of a solid state image pickup device in the present invention wherein (a) is a cross sectional view and (b) is a plan view.

Fig. 2 is a equivalent circuit drawing of the example.

Fig. 3 is a usual circuit drawing of MOS type solid state image pickup device.

101---substrate
103---gate electrode
105---vertical line
107---lower electrode
108---receptive thin film
109---oxidation film
110---upper electrode

Applicant Suwa seiko-sha
Attorney Tsutomu Mogami

⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　昭61－141174

⑤1Int.Cl.⁴	識別記号	庁内整理番号	④3公開 昭和61年(1986)6月25日
H 01 L 27/14		7525－5F	
H 04 N 5/335		8420－5C	

審査請求 未請求 発明の数 1 (全4頁)

⑤4発明の名称　固体撮像装置

②1特　願　昭59－263366

②2出　願　昭59(1984)12月13日

⑦2発明者　竹下　哲義　諏訪市大和3丁目3番5号　株式会社諏訪精工舎内

⑦2発明者　栗原　一　諏訪市大和3丁目3番5号　株式会社諏訪精工舎内

⑦2発明者　岡　秀明　諏訪市大和3丁目3番5号　株式会社諏訪精工舎内

⑦2発明者　長谷川　和正　諏訪市大和3丁目3番5号　株式会社諏訪精工舎内

⑦1出願人　セイコーエプソン株式会社　東京都新宿区西新宿2丁目4番1号

⑦4代理人　弁理士　最上　務

明　細　書

1　発明の名称

固体撮像装置

2　特許請求の範囲

(1)　絶縁性基板上に形成した受光素子の蓄積放電電荷量を検出する形式の固体撮像装置において該受光素子の下部電極の一部を酸化することで上部電極との間に該受光素子と並列に容量を設けたことを特徴とする固体撮像装置。

(2)　受光素子として非晶質シリコン、そして下部電極にクロムもしくはアルミニウムを用いた受光素子で、非晶質シリコンのフォトニッチングと同時に酸化膜の付加容量部分を形成することを特徴とする特許請求の範囲第1項記載の固体撮像装置。

3　発明の詳細な説明

(産業上の利用分野)

本発明は、固体撮像素子を用いた固体撮像装置に関するものである。

(従来の技術)

従来、固体撮像素子としてCCD型やMOS型が実用化されている。固体撮像素子は撮像管に比べて振動や衝撃に強く、消費電力が少なく、長寿命であるなどの特徴がある。さらに、CCD型とMOS型を比べると、MOS型はCCD型より開口率が大きくできて、転送電荷量の制限がないので大きな信号量が取り出せる。しかし、MOS型は雑音が大きいという欠点を有する。第3図に代表的なMOS型の回路構成図をのせる。この図を用いて雑音の発生原因をのべると、最大の問題は水平MOSアナログスイッチの開閉にともなう雑音であり、これは垂直ラインV_1～V_nの配線容量ができ、さらにV_1～V_nについているトランジスタの電極－基板容量が大きいためにラインに残っている雑音電荷を読み出してしまうことにある。これらは、受光部の容量に比べてはるかに大きいことのS/Nの大きな低下につながる。以上の

雑音の点に解決しなければならない問題点がある。これはCCDだけでなくMOSでも同じでその原因の一つに受光部以外に入射した光による電荷が信号ラインに混入することによる。

そこで、本発明は絶縁物を用いて素子を薄膜化することで配線容量を大きく低減させ、さらに受光素子に付加容量を設けてS/N比を上げる方法が考えられる。たとえば、付加容量としてSiO_2やY_2O_3などの薄膜を新たに設ける方法がある。

〔発明が解決しようとする問題点〕

しかし前述の従来技術では受光素子に付加容量を形成するのに新たに薄膜を設けてやらねばならないために製造工程が増えてしまいコストが増加するとともに、薄膜が均一に形成されにくいために雑音に結びつくことになる。

そこで本発明はこのような問題点を解決するもので、その目的とするところは、製造工程を増やすことなく均一な付加容量を受光素子に並列に設けた固体撮像装置を提供するところにある。

〔問題点を解決するための手段〕

本発明の固体撮像装置は、受光素子部分をマトリクスとして受光素子の下部電極の一部を酸化することで形成される酸化膜が上部電極との間で付加容量とすることで、容易に均一な付加容量が受光素子と並列に設けることができることを特徴とする。

具体には受光素子のフォトエッチングに酸素含有のフレオンガスを用いたドライエッチング技術を用いることで必然的にできる酸化膜を利用する。また、受光素子部分に非晶質シリコンを用い、ドライブ部分に多結晶シリコンを用いることでスミアの少ない高感度かつ飽和光量の大きい固体撮像素子となる。

〔作用〕

本発明の上記の構成によれば、受光素子の下部電極に形成される酸化膜が下部電極と上部電極の間で素子の付加容量となり、飽和光量を増すとともに高S/N比の低雑音固体撮像素子となる。

〔実施例〕

第1図は、本発明の実施例における構造図である。受光素子及びスイッチング素子は半導体薄膜ならばいかなるものでも利用は可能であるが、ここでは受光素子として非晶質シリコンのフォトダイオード、スイッチング素子として多結晶シリコンTFTを用いて代表させる。第2図は第1図の等価回路である。第1図において(a)は断面図、(b)は平面図であり、製造工程としては以下に示す様になる。石英ガラスなどの絶縁基板101上にNドープの多結晶シリコン膜102を形成、熱酸化法でゲート絶縁膜を形成後にゲート電極となる第2の多結晶シリコン膜103を形成する。これはまたゲート・ラインともなる。その後にイオン打込み法によりソースとドレイン電極を設ける。次に層間絶縁膜104としてSiO_2などを形成した後、コンタクトホールを形成し垂直ライン105をAlなどの導電性物質で形成し、その上に層間絶縁膜を覆わて平坦化のためにポリイミド樹脂膜を106として形成する。以上は一般的な多結晶ポリシリコンTFTの形成方法であり、これから後が本発明に関して重要な製造工程である。層間絶縁膜にコンタクトホールを形成した後に画素の下部電極としてCrやAlなどで導電性薄膜107を形成するが、ここでこの薄膜は108の受光膜を形成後にこの受光膜（ホトレジストがついている場合もあるリをリフトオフして107の導電性薄膜を酸化して付加容量部109とするため、酸化が容易で酸化膜が高抵抗で緻密でなくてはならない。酸化方法としては種々の方法が考えられるが、108の受光薄膜を酸素とフレオンのプラズマでエッチングする場合は必然的に酸化膜109が形成され、なんら酸化工程を増やす必要はない。この方法で酸化した後にさらに酸素プラズマ処理したり、熱酸素などで酸化してもよく、水蒸気酸化などもよい。本実施例でこれらの酸化方法でCrとAl-Siを下部電極107とした場合の特性例を第1表に示す。ここで、108の受光薄膜はOコプラズマCVD法で形成した非晶質シリコン（以下、a-Siと略す）、110は透明電極（上部電極）ならばいかなるものでもよいが、ここではITOを用いている。

条　件	電子容量(×10⁶/100 μm²)	絶縁性
(1) $CF_4 + O_2$ で a-Si をエッチング	0.2	良
(2) (1)に加えて O_2 プラズマ処理	0.5	最　良
(3) (1)に加えて熱硫酸処理	0.5	良
(4) 電極に Al-Si を用い (2)の条件	0.7	並
(5) 電極に Al-Si を用いて水蒸気で酸化	0.3	良

注) (1)～(3)の下部電極は Cr である。

第 1 表

第 1 表で電子容量は a-Si の容量と酸化膜の付加容量との和であるが、a-Si の容量は 0.01 pF/100 μm² 程度である。均一性に関しては、(3)の条件がもっとも良く全電子でのバラツキは ±1 % 以内であり、他は ±2.5 % 以内である。いずれにしてもこれらは SiO_2 や誘電薄膜を別途に形成する場合よりも著しく容易であり、バラツキも少ない (SiO_2 の場合は ±5 % 程度)。

第 2 図の等価回路でみると、以下の工程により生じた電子 Di に付加容量 Co が並列についた回路となる。

また上記例では下部電極として金属をあげたが不純物ドーピングされた低抵抗非晶質シリコンを用いて、酸化をうけない SiO_2 を形成して付加容量として用いることもできる。

(発明の効果)

以上述べたように本発明によれば、画像を受けた電子のパターンをマスクとすることで製造工程を増やすことなく、著しく容易に均一性の高い付加容量を形成できるために S/N 比が大きく、解像力の大きいすぐれた固体撮像装置を低コストで容易に得ることができる。

4. 図面の簡単な説明

第 1 図は本発明の固体撮像装置の実施例であり、(a)は断面図で、(b)は平面図である。

第 2 図は実施例の等価回路図である。

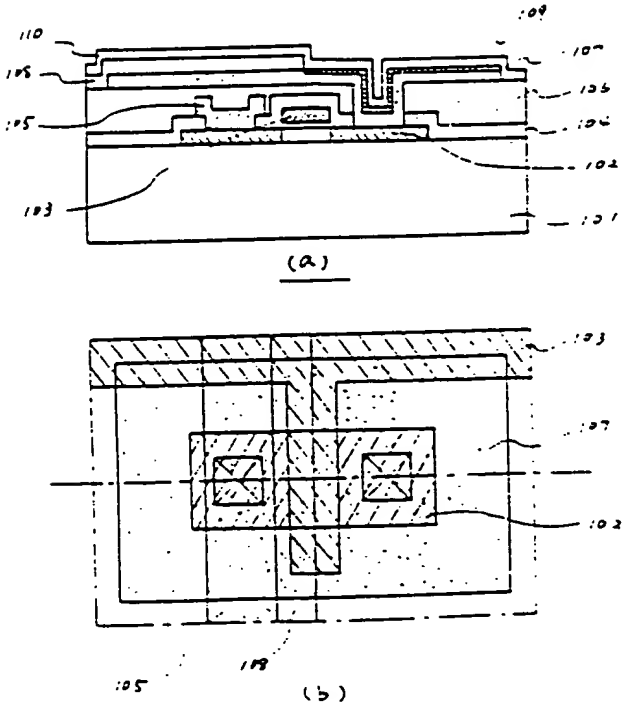
第 3 図は一般的な MOS 型固体撮像装置の回路図である。

101 …… 基板
103 …… ゲート電極
105 …… 垂直ライン
107 …… 下部電極
108 …… 受光部薄膜
109 …… 酸化膜
110 …… 上部電極

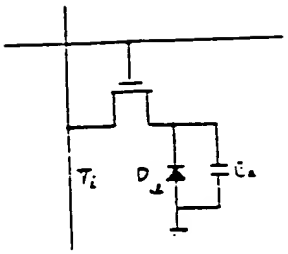
以　上

出願人　株式会社　諏訪精二舎

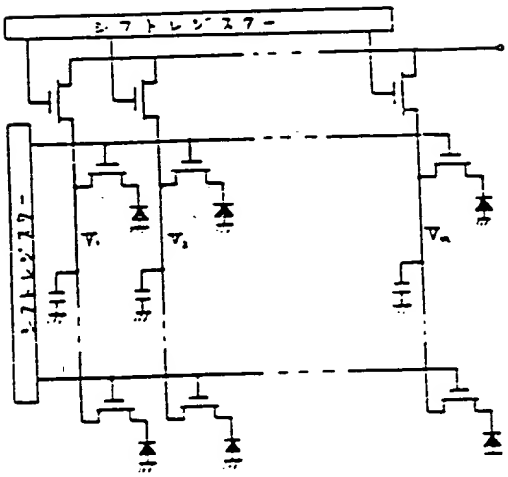
代理人　弁理士　最　上　務



第 1 図



第 2 図



第 3 図